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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,894	08/28/2001	Christoph Dominique Loeffler-Lejeune	716-055us	7829

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EXAMINER	
HAN, CLEMENCE S	
ART UNIT	**PAPER NUMBER**
2665	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,894	LOEFFLER-LEJEUNE, CHRISTOPH DOMINIQUE	
	Examiner	Art Unit	
	Clemence Han	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 15-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/28/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: In the section of Brief Description of the Drawings, Fig. 4 depicts input port in the switch depicted in not Fig. 4 but Fig. 3 and Fig. 6 depicts the subtasks of not task 503 but task 502.

Appropriate correction is required.

Claim Objections

2. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Claim 14 is missing.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 9, 10 and 15-17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 9, 15 and 16 contains the limitation of the controller storing value in the write pointer based on the contents of the register. This limitation is not described in the specification (see Figure 4).

5. Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 13 recites two second memories storing the second signal. This limitation is not described in the specification (see Figure 4).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claim 1-13 and 15-17 are rejected under 35 U.S.C. 102(a) as being anticipated by Kusyk (US 6,246,668).

Regarding to claim 1, Kusyk teaches an integrated circuit (see Figure 5) comprising: a first input port 41a for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries 31a; a second input port 42b for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries 32b; a first frame position register whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time (H1); and a second frame position register whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time (H2) (Column 7 Line 62-64 and Column 5 Line 30-32).

Regarding to claim 2, Kusyk teaches a first memory 67 that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer 57 and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer 61; and a second memory 68 that stores said second time-division multiplexed signal at a location that is indicated by a second

write pointer 58 and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer 62.

Regarding to claim 3, Kusyk teaches a first retimer 37 for retiming said first time-division multiplexed signal; and a second retimer 38 for retiming said second time-division multiplexed signal.

Regarding to claim 4, Kusyk teaches an output port 35; and a cross-connect 15 for outputting at least a portion of said first time-division multiplexed signal via said output port.

Regarding to claim 5, Kusyk teaches a method comprising: receiving a first time-division multiplexed signal that comprises a first series of frame boundaries 31a; receiving a second time-division multiplexed signal that comprises a second series of frame boundaries 32b; indicating, at a point in time, how far said first time-division multiplexed signal is from a frame boundary; and indicating, at said point in time, how far said second time-division multiplexed signal is from a frame boundary (Column 7 Line 62-64 and Column 5 Line 30-32).

Regarding to claim 6, Kusyk teaches storing said first time-division multiplexed signal into a first memory 67 at a location that is indicated by a first write pointer 57; reading said first time-division multiplexed signal from a location in said first memory that is indicated by a first read pointer 61; storing said

second time-division multiplexed signal into a second memory 68 at a location that is indicated by a second write pointer 58; and reading said second time-division multiplexed signal from a location in said second memory that is indicated by a second read pointer 62.

Regarding to claim 7, Kusyk teaches retiming said first time-division multiplexed signal in accordance with a clock signal 39; and retiming said second time-division multiplexed signal in accordance with said clock signal (Column 8 Line 8-18, see Figure 2 and 5).

Regarding to claim 8, Kusyk teaches an apparatus comprising: a first integrated circuit comprising: (i) a first input port 41a for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries 31a; (ii) a second input port 42b for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries 32b; (iii) a first frame position register whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time (H1); and (iv) a second frame position register whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time (H2) (Column 7 Line 62-64 and Column 5 Line 30-32); and a second integrated circuit

comprising a controller 43a for reading the contents of said first frame position register and said second frame position register (Column 8 Line 12-14).

Regarding to claim 9, Kusyk teaches a first memory 67 that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer 57 and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer 61; and a second memory 68 that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer 58 and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer 62.

Regarding to claim 10, Kusyk teaches an output port 35; and a cross-connect 15 for outputting at least a portion of said first time-division multiplexed signal via said output port.

Regarding to claim 11, Kusyk teaches a composite switch comprising: a first integrated circuit comprising: a first input port 41a for receiving a first time-division multiplexed signal that comprises a first series of frame boundaries 31a; a first frame position register whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a point in time (H1) (Column 7 Line 62-64 and Column 5 Line 30-32); and a second integrated circuit comprising: a second input port 42b

for receiving a second time-division multiplexed signal that comprises a second series of frame boundaries 32b, and a second frame position register whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said point in time (H2) (Column 7 Line 62-64 and Column 5 Line 30-32); and a controller 43a for reading the contents of said first frame position register and said second frame position register.

Regarding to claim 12, Kusyk teaches a third integrated circuit 21, 22 for outputting said first time-division multiplexed signal to said first integrated circuit 17 and for outputting said second time-division multiplexed signal to said second integrated circuit 18.

Regarding to claim 13, Kusyk teaches a memory 68 that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer 58 and that reads said second time-division multiplexed signal at a location that is indicated by a second read pointer 62.

Regarding to claim 15, Kusyk teaches controller 43a.

Regarding to claim 16, Kusyk teaches the first, second and third integrated circuit as shown in the rejection of claim 11 and 12. The fourth integrated circuit contains the same component as the second and the third integrated circuit and

connected to the second and the third integrated circuit. Kusyk teaches such integrated circuit 10 connected to the other integrated circuit 10' with same function (see Figure 1).

Regarding to claim 17, Kusyk teaches said first point in time and said second point in time are the same (Figure 2B).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clemence Han whose telephone number is (571) 272-3158. The examiner can normally be reached on Monday-Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. H.

Clemence Han
Examiner
Art Unit 2665

STEVEN NGUYEN
PRIMARY EXAMINER